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10/579,911	04/09/2007	Satoru Hanzawa	XA-10573	6903

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EXAMINER	
HIDALGO, FERNANDO N	
ART UNIT	PAPER NUMBER
2827	

NOTIFICATION DATE	DELIVERY MODE
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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

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Office Action Summary	Application No.	Applicant(s)	
	10/579,911	HANZAWA ET AL.	
	Examiner	Art Unit	
	FERNANDO N. HIDALGO	2827	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *09 April 2007*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *11-19* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *11-19* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *09 April 2007* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date *4/9/07*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Drawings

1. Figures 21 and 22, disclosed as prior art on pages 1-3 of the specification should be designated by a legend such as --Prior Art-- because only that which is old is illustrated. See MPEP § 608.02(g). Corrected drawings in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. The replacement sheet(s) should be labeled "Replacement Sheet" in the page header (as per 37 CFR 1.84(c)) so as not to obstruct any portion of the drawing figures. If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

Claim Objections

2. Claim(s) 1 is objected to because of the following informalities: lines 14-15 of the claim site "the comparator has **the first** and **the second** MOS transistors" (emphasis added). There is no antecedent fro the first and second transistors. For purposes of advancing examination, the following interpretation will be used: a first and a second MOS transistors. Appropriate correction is required.

3. **Claim(s) 1-10**, cancelled by applicant.

Claim Rejections - 35 USC § 112

4. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

5. **Claim (s) 17** recites the limitation "the first and the second coupling capacitance" and “the contacts” in lines 3-5. There is insufficient antecedent basis for this limitation in the claim. Furthermore, Claim(s) 17 is rejected under 35 U.S.C. 112, second paragraph, as being incomplete for omitting essential structural cooperative relationships of elements, such omission amounting to a gap between the necessary structural connections. See MPEP § 2172.01. The omitted structural cooperative relationships are: lines 3-5 claim a coupling parasitic capacitance "between the search lines and the first match lines are generated principally by the contacts." As well known, a capacitive structure is formed by the intersection of at least two conductive planes, such as the search lines and the first match line; however, a coupling capacitance "generated principally by the contacts” omits structural cooperative relationships between the search lines and the first match line on the one hand, and "the contacts" on the other hand. Is one to interpret that "the contacts" contact the search lines and the first match line? Since, for example FIG. 1 of the instant invention illustrates that there is no direct electrical connection between the search lines and the first match lines; it is highly ambiguous what role “the contacts,” as claimed, play.

Claim Rejections - 35 USC § 103

6. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

7. **Claim(s) 11 and 12** are rejected under 35 U.S.C. 103(a) as being unpatentable over U.S. Patent No. 6343029 B1 to Kengeri et al. ("Kengeri") in view of U.S. Publication 66MHz 2.3M Ternary Dynamic Content Addressable Memory to Lines et al. ("Lines").

As to **claim 11**, Kengeri discloses a semiconductor integrated circuit device wherein each of the match line pairs has a precharge circuit (FIG. 1 shows each of the match line pairs ML and SL have pre-charge circuits 181 and 182, respectively); the precharge circuit drives the first match line of the match line pair to the first voltage and the second match line thereof to the second voltage lower than the first voltage, respectively (FIG. 1 shows that first pre-charge circuit 181 drives match line ML to first voltage Vc and second pre-charge circuit drives match line SL to GND, which is lower than the first voltage, respectively); each of the memory cells has a storage circuit and a comparator (FIG. 1 shows storage circuit 191 and comparator 110; also see Column 2, lines 52-65); each of the comparators has the first and the second MOS transistors (FIG. 4 shows comparator 110 having a first and a second MOS transistors 113, 114); gate electrodes of the first and second MOS transistors are connected to the search lines, respectively (FIG. 4 shows that gates of 113 and 114 are connected to search lines DLA and DLB, respectively); and the second match line is put in a floating state when comparison operation is performed in the comparator (FIG. 1, Column 1, lines 47-67 disclose that the second latch line SL is put in a floating state when in comparison operations; that is disclosed is that

SL is pre-charged to ground, prior to a comparison operation, and in response to a data mismatch detected by the comparator, the first match line voltage is put on charge-sharing with the SL match voltage, as pre-charged, and consequently the first match voltage is prevented to discharge to ground. This discharge to ground, inherently, can only happen if the second match line had been connected to ground; charge sharing can only take place between two signal voltages able to drive one-another).

Kengeri does not expressly disclose a plurality of match line pairs, a plurality of search line pairs intersecting the plurality of match line pairs, and a plurality of memory cells arranged at intersecting points of the plurality of match line pairs with the plurality of search line pairs; either of source or drain electrodes of the first and second MOS transistors are connected to the first match line.

Lines teaches a plurality of match line pairs (FIG. 2 shows a memory cell with a pair of match lines, and FIG. 1 shows an exemplary memory array floor plan of the memory cells in FIG. 2; thus a plurality of match lines), a plurality of search line pairs intersecting the plurality of match line pairs (FIG. 2 shows a memory cell with a pair of search lines, and FIG. 1 shows an exemplary memory array floor plan of the memory cells in FIG. 2; thus a plurality of search lines), and a plurality of memory cells arranged at intersecting points of the plurality of match line pairs with the plurality of search line pairs (FIG. 2 shows a memory cell arranged with a pair of match lines and search lines, and FIG. 1 shows an

exemplary memory array floor plan of the memory cells in FIG. 2; thus a plurality of cells arranged as in FIG. 2; alternatively FIG. 3 shows a plurality of memory cells as in FIG. 2); either of source or drain electrodes of the first and second MOS transistors are connected to the first match line (FIG. 2 shows a memory cell, wherein the source/drain of the first and second MOS transistors M3, M5 are connected to the first match line ML).

Kengeri and Lines are analogous art because they are from the same field of endeavor regarding semiconductor memory circuit design, more specifically Content addressable memory.

At the time of invention, it would have been obvious to a person of ordinary skill in the art to provide a plurality of match line pairs, a plurality of search line pairs intersecting the plurality of match line pairs, and a plurality of memory cells arranged at intersecting points of the plurality of match line pairs with the plurality of search line pairs; either of source or drain electrodes of the first and second MOS transistors are connected to the first match line as taught by Lines in the above claim limitation rejection. The suggestion/motivation would have been obvious to one of ordinary skill in the art in providing a memory array comprising a plurality of memory cells; while Kengeri discloses his invention with a cell as the focal point, it is obvious to one of ordinary skill that practical realization of the invention encompasses a memory array device. Furthermore, Kengeri' comparator and Lines' comparator cell differ only in the match line that is connected to the first and second MOS transistors. One advantage Lines has

with his comparator is that first and second MOS transistors de-couple the devices driven by the storage cells from a dynamically operational first match line, as influenced by search line dynamic activity. This inherently reduces the coupling of the storage cells with the dynamically changing first match line and thus prevents undue charge influence on the storage elements from dynamic changes on the first match line.

Therefore, it would have been obvious to combine Kengeri with Lines to make the above modification.

As to **claim 12**, Kengeri discloses that a source - drain path in the first MOS transistor is included in the first current path between the first and the second match lines (FIG. 1 shows that source/drain of the first transistor 113 is included in the first current path between first match line ML and second match line SL); a source - drain path in the second MOS transistor is included in the second current path between the first and the second match lines (FIG. 1 shows that source/drain of the second transistor 114 is included in the second current path between first match line ML and second match line SL); the comparator generates a signal voltage corresponding to a result of comparing data stored at the storage circuit and data inputted via the search lines at the match line (FIG. 1 shows that in response to data inputted on the search lines DLA and DLB and data stored on storage circuits 191 and 192, comparator 110 generates signal voltage on first match line ML).

8. **Claim(s) 13-16, and 18-19** are rejected under 35 U.S.C. 103(a) as being unpatentable over U.S. Patent No. 6343029 B1 to Kengeri et al. ("Kengeri") in view of U.S. Publication 66MHz 2.3M Ternary Dynamic Content Addressable Memory to Lines et al. ("Lines"), further in view of U.S. Patent No. 6483733 B2 to Lines et al. ("Lines-2").

As to **claim 13**, Kengeri, as modified, discloses substantially the claimed invention except that the first and the second coupling capacitances being parasitic between the search line and the first match line are larger than the third and the fourth coupling capacitances being parasitic between the search line and the second match line.

Lines-2 teaches that the first and the second coupling capacitances being parasitic between the search line and the first match line are larger than the third and the fourth coupling capacitances being parasitic between the search line and the second match line (FIG. 2 shows an exemplary memory cell and comparator having a first match line ML, a second match line DL and first and second search lines SL1 and SL2; FIG 6B shows a circuit mask layout of FIG. 2, wherein it is shown that the parasitic capacitance (not shown, but inherently available and thus operable to be analyzed) between the first match line ML and the search line SL2 is larger than the parasitic capacitance between the second match line DL and the search line SL2as follows: the first match line ML is much closer in proximity to search line SL2 resulting in a larger parasitic capacitance, the proximity of the second match line to the search line is plainly observable to be not as close, thus resulting in a smaller coupling parasitic capacitance; as well

known in the art, capacitance is inversely proportional to the distance between two conductive elements).

For suggestion/motivation to combine, see rejection to claim 11.

As to **claim 14**, Kengeri, as modified, discloses substantially the claimed invention except a match detector is arranged in each of the second match lines; and the match detector determines the data-comparison results by discriminating voltages of the second match line.

Lines teaches a match detector is arranged in each of the second match lines; and the match detector determines the data-comparison result by discriminating voltages of the second match line (FIG. 4 shows a match detector sense amplifier circuitry, wherein the match line ML voltage, as it changes depending on a match or mismatch, determines the result from the comparator of FIG. 2 by noticing differences, discriminating voltages on the second match line as follows: as seen on FIG. 2, the comparison result of the comparator as available on the first match line ML, is highly dependent on the voltage value expectancy of the second match line ML_VSS; depending on a data match or mismatch, the first mach line voltage value will reach a value by discriminating the value of the second match line via devices M3-M6).

For suggestion/motivation to combine, see rejection to claim 11; further, it would have been obvious to provide a means to detect to comparison value as generated by the cell/comparator for amplification and further data processing as well done and practiced in applications using memory devices in general.

As to **claim 15**, Kengeri, as modified, discloses substantially the claimed invention except that the storage circuit has two transistors and two capacitors.

Lines teaches that the storage circuit has two transistors and two capacitors (FIG. 2 shows two transistors M1 and M2 and two capacitors C1 and C2).

Kengeri and Lines are analogous art because they are from the same field of endeavor regarding semiconductor memory circuit design, more specifically Content addressable memory.

At the time of invention, it would have been obvious to a person of ordinary skill in the art to provide that the storage circuit has two transistors and two capacitors as taught by Lines in the above claim limitation rejection. The suggestion/motivation would have been to use DRAM technology for the basic cell to provide large density memory in a comparably reduced semiconductor area (See Abstract).

Therefore, it would have been obvious to combine Kengeri with Lines to make the above modification.

As to **claim 16**, see rejection to claim 11, furthermore, Kengeri discloses that the comparator comprises the first and the second MOS transistors connected serially so as to form the first current path between the first and the second match lines (FIG. 1 shows first and second MOS transistors 111 and 113 between the first match line ML and second match line SL forming a current path), and the third and the fourth MOS transistors connected serially so as to

form the second current path (FIG. 1 shows third and fourth MOS transistors 112 and 114 between the first match line ML and second match line SL forming a second current path).

Lines teaches gate electrodes of the first and third MOS transistors are connected to the search lines, respectively (FIG. 2 shows that first and third MOS transistors M3 and M5 have gates connected to search lines SL1bb and SL2b, respectively); either of electrodes of source or drain electrodes of the first and the third MOS transistors are connected to the first match lines through contacts formed through self- aligned process (FIG. 2 shows drain/source of first and third MOS transistors connected to first match line ML by making use of DRAM technology which enables a smaller memory cell foot-print, see Abstract); gate electrodes of the second and fourth MOS transistors are connected to the storage circuits, respectively (FIG. 2 shows gate electrodes of the second and fourth MOS transistors M4 and M6 connected to storage elements C1 and C2, respectively); and either of electrodes of source or drain electrodes of the second and fourth MOS transistors are connected to the second match lines through contacts formed through self- aligning process (FIG. 2 shows that drain/source of second and fourth MOS transistors are connected to second match line by making use of DRAM technology which enables a smaller memory cell foot-print, see Abstract)

Alternatively Lines-2 teaches a memory cell (FIG. 2) wherein first and third MOS transistors connect to the first match line ML and second and fourth MOS transistors connect to second match line DL also using DRAM technology

Additionally, please refer to Chapter 2100 of the MPEP:

2113 [R-1] Product-by-Process Claims

PRODUCT-BY-PROCESS CLAIMS ARE NOT LIMITED TO THE MANIPULATIONS OF THE RECITED STEPS, ONLY THE STRUCTURE IMPLIED BY THE STEPS

"[E]ven though product-by-process claims are limited by and defined by the process, determination of patentability is based on the product itself. The patentability of a product does not depend on its method of production. If the product in the product-by-process claim is the same as or obvious from a product of the prior art, the claim is unpatentable even though the prior product was made by a different process." *In re Thorpe*, 777 F.2d 695, 698, 227 USPQ 964, 966 (Fed. Cir. 1985) (citations omitted) (Claim was directed to a novolac color developer. The process of making the developer was allowed. The difference between the inventive process and the prior art was the addition of metal oxide and carboxylic acid as separate ingredients instead of adding the more expensive pre-reacted metal carboxylate. The product-by-process claim was rejected because the end product, in both the prior art and the allowed process, ends up containing metal carboxylate. The fact that the metal carboxylate is not directly added, but is instead produced in-situ does not change the end product.).

ONCE A PRODUCT APPEARING TO BE SUBSTANTIALLY IDENTICAL IS FOUND AND A 35 U.S.C. 102 /103 REJECTION MADE, THE BURDEN SHIFTS TO THE APPLICANT TO SHOW AN UNOBVIOUS DIFFERENCE

"The Patent Office bears a lesser burden of proof in making out a case of *prima facie* obviousness for product-by-process claims because of their peculiar nature" than when a product is claimed in the conventional fashion. *In re Fessmann*, 489 F.2d 742, 744, 180 USPQ 324, 326 (CCPA 1974). Once the examiner provides a rationale tending to show that the claimed product appears to be the same or similar to that of the prior art, although produced by a different process, the burden shifts to applicant to come forward with evidence establishing an unobvious difference between the claimed product and the prior art product. *In re Marosi*, 710 F.2d 798, 802, 218 USPQ 289, 292 (Fed. Cir. 1983) (The claims were directed to a zeolite manufactured by mixing together various inorganic materials in solution and heating the resultant gel to form a crystalline metal silicate essentially free of alkali metal. The prior art described a process of making a zeolite which, after ion exchange to remove alkali metal, appeared to be "essentially free of alkali metal." The court upheld the rejection because the applicant had not come forward with any evidence that the prior art was not "essentially free of alkali metal" and therefore a different and unobvious product.).

As to **claim 18**, see rejection to claim 1; furthermore, Kengeri discloses that the comparator (FIG. 1, 110) is connected to one of the search lines (FIG. 1, search line pairs (FIG. 1, DLA, DLB) and one of the first match lines (FIG. 1, first match line ML); the comparator is inserted between the plurality of match line pairs to compare data held at the storage circuit and data inputted via the plurality of search lines (FIG. 1 shows comparator 110 inserted between match lines ML and SL to compare data held at storage circuit 191, 192 and data inputted via plurality of search lines DLA, DLB).

Lines-2 and/or Lines teach a plurality of bit line pairs parallel to the plurality of search line pairs (FIG. 2 of Lnes-2 shows bit lines BL1-BL2 in parallel to search lines SL1-SL2; FIG. 2 of Lines also shows similarly, alternatively).

Lines-2 teach that the voltage amplitude of the plurality of bit line pairs is larger than that of the plurality of search line pairs (FIG. 3A and Column 6, lines 15-31 teach that the search lines SL1 and SL2 are both held at Low level voltage, while bit line BL1, BL2 voltage potential, as shown in FIG. 3A is high, correspondingly to the complementary data written).

At the time of invention, it would have been obvious to a person of ordinary skill in the art to provide a plurality of bit line pairs parallel to the plurality of search line pairs; and that the voltage amplitude of the plurality of bit line pairs is larger than that of the plurality of search line pairs as taught by Lines and Lines-2 in the above claim limitation rejection. While Kengeri does not expressly disclose bit lines complementing his memory cell -disclosing a broader CAM storage cell at large- it is obvious to one of ordinary skill in the art to expect that bit lines for writing/reading data to/from the memory cells are part and parcel of a memory device having any utility in an application. As such, it would have been obvious to one of ordinary skill in the art to complement the teachings of Lines and Lines-2 with those of Kengeri.

Therefore, it would have been obvious to combine Kengeri with Lines and Lines-2 to make the above modification.

As to **claim 19**, Kengeri discloses substantially the claimed invention except that each of the storage circuits has two transistors and two capacitors.

Lines and Lines-2 teach that each of the storage circuits has two transistors and two capacitors (FIG. 2 of Lines shows that the storage circuit has

two transistors M1, M2 and two capacitors C1, C2; alternatively and similarly Lines-2 teaches at FIG. 2 similar storage circuit: T1-T2 and C1-C2).

For suggestion/motivation to combine, see rejection to claim 18.

Conclusion

9. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. U.S. Publication No. 2003/0058672 A1 to Aikawa regarding an associative memory circuit with search data and U.S. Patent No. 6400594 B2 to Hata regarding content addressable memory having match lines.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to FERNANDO N. HIDALGO whose telephone number is (571)270-3306. The examiner can normally be reached on Monday-Friday, 7:30AM-5:00PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Amir Zarabian can be reached on 571-272-1852. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/Fernando N. Hidalgo/
Examiner, Art Unit 2827

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